

INTRODUCTION: THE PCI-OPPORTUNITY

Hewlett Packard has announced a unique new development tool for developers of PCI chips, cards and systems.

The Peripheral Component Interconnect (PCI) bus is the new performance standard in the world of PC and workstation peripheral busses and has been developed for high speed data transfer, for example for real-time multimedia applications and high speed disk storage solutions.

The HP E2910A, 33MHz PCI Bus Exerciser emulates the bus traffic of absent PCI devices with complete control over protocol variations. It allows semiconductor and computer manufacturers to cut several weeks off product development schedules by accelerating the debugging process.

The new bus exerciser brings up, debugs and validates PCI designs. It simulates devices with bus traffic, as master or target, emulating the real PCI environment of the final product. From ASIC emulation and prototype hardware, through BIOS/driver development, to integration and validation you can save exhaustive verification time, and make your PCI device available sooner.

The PCI developer records, modifies and replays real traffic to reproduce and isolate problems fast. The HP E2910A provides continuous protocol monitoring in real-time so that your customers never overlook protocol violations. By using the various listers which filter and disassemble PCI traffic, any user can quickly analyze and identify problems at the PCI level. Together with the HP 16500B logic analyzer the PCI bus exerciser turns a standard PC into a powerful exercising and analyzing tool for 32- and 64-bit PCI bus systems.

The customer has a choice of PCI adapters for in-system and card test.

MS Windows and two free ISA slots (for the HP-IB card and the test sequencer card of the E2910A) are required in the PC.

KEY FEATURES

- * Generates all PCI transactions (including reserved), as master or target as required.
- * Full protocol participation 0 - 33 MHz
- * Complete control over protocol variations/corner cases, for example:
 - Wait cycles
 - Burst length
 - Terminations (Abort, disconnect, retry)
 - Parity and error reporting
- * Real-time continuous monitoring detects protocol violations.
- * Pattern recognizer and Test sequencer for complex triggering and branching of PCI transaction sequences.
- * Windows based User Interface with:
 - PCI Bus Transaction editor for defining transactions.
 - Sequence editor for defining transaction sequences with trigger/branching.
 - Pattern Editor for defining trigger/branching conditions combining bus signals, bus states, protocol violations.

- * Software integrates HP 16500B Logic Analyzer to capture bus traffic.
- * Hierarchical listers disassemble bus traffic for easy, meaningful analysis:
 - Bus cycle lister (Address B8000, wait no TRDY, data xxB6xxxx, idle idle).
 - Bus Transaction lister (Mem Write B8000, data xxB6xxxx).
 - Configuration lister interprets configuration commands.
- * Record, edit and replay of PCI transactions.
- * Adapters for 32/64 Bit In-system test at PCI connector, or for add-in card test.

CONTRIBUTIONS

The PCI bus exerciser accelerates the development of PCI devices and systems (chips, cards, motherboards and systems):

- * Fast, comprehensive verification of PCI functionality
 - All transactions, exceptions
- * Emulation of missing devices by emulating their traffic on the bus
 - Parallel development/verification of different devices, and low level software before system integration
 - Early start to system integration
- * Accelerated debug/verification
 - Generate stressful traffic
 - Easy analysis of bus traffic
 - record and deterministic replay of suspect traffic causing intermittent problems gets you to the root cause faster
 - Known PCI reference helps to point the finger
- * Applicable throughout development process
 - hardware emulation
 - first hardware bring-up
 - system integration and troubleshooting
 - validation