What Makes Bit-Error Ratio Testing With Integrated CDR Beneficial?

by Michael Fleischer, Agilent Technologies

The intention of this TechNote is to show the necessity of using clock data recovery (CDR) in conjunction with a bit-error ratio tester (BERT) and the advantages of integrating it into the BERT error detector (ED). Furthermore, it will discuss why this CDR should have adjustable parameters.

BERTs were built decades ago without integrated CDRs to be mainly used in communication applications. The signal for the BERT error detector clock input could either be taken from the BERT pattern generator (PG), or was supplied by the device-under-test (DUT) or, sometimes, by an external golden phase-locked loop (PLL)/CDR circuit (see Fig. 1). As the DUTs were mainly targeting SONET systems, the variety of different PLLs that was required was low and did not change rapidly. The industry didn't expect the development of highly-integrated test equipment, and to design an appropriate and very often complex test set up was seen as an art, and a differentiating factor between competitors, not just as an obstacle to bringing a part to market.

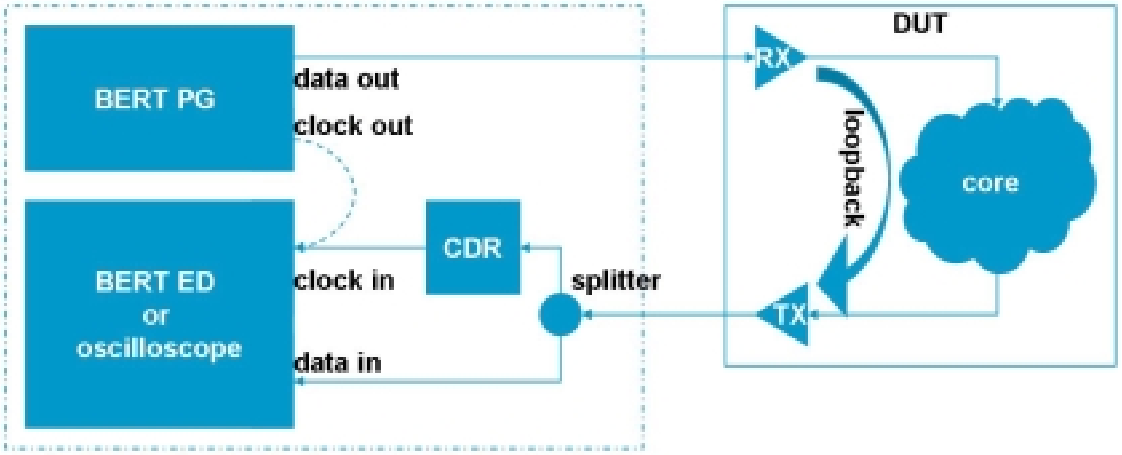


Fig. 1: Block Diagram

The advent of serial technologies in computer busses caused these conditions to drastically change. Different standards rapidly arose each with its own set of data rates and architectures. New clocking schemes such as spread spectrum clocking (SSC) were deployed. Designers, typically with a digital background, were suddenly confronted with the need to test physical layer parameters at very high data rates, where an RF background would be helpful. They demanded to get reliable results in a short time without having to become an RF measurement expert.

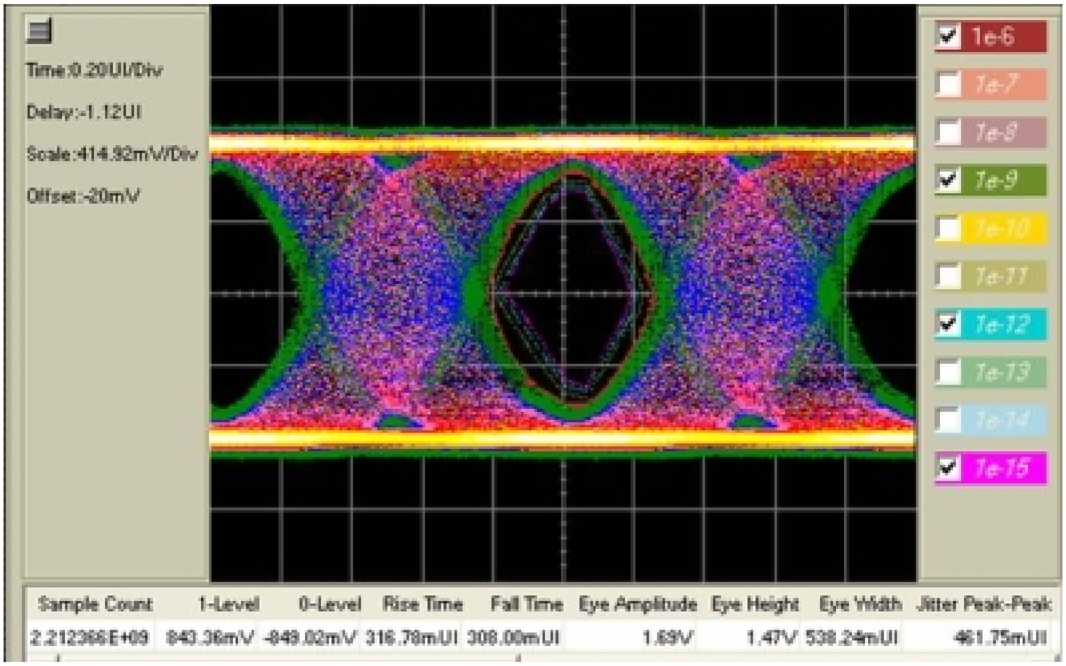
In these computer buses, clocks are typically embedded in the data stream and the DUTs do not supply a clock for the BERTs ED and in case of SSC due to the delay between (seen from the BERT) outgoing and incoming data, the BERT PG clock cannot be used.

When analyzing typical BERT measurements for different testing scenarios, more often for an overall system performance check against a maximum BER, it is found that a BERT is used for characterization of system components and/or modules, such as a transmitter (Tx), receiver (Rx) or line cards.

Rx testing: A Rx usually needs to be characterized for its tolerance of signal perturbations generated by the Tx itself, neighboring Txs (in the form of crosstalk) or the channel (in form of ISI), often summarized as Jitter Tolerance Test.

The BERT PG is used to stimulate the Rx with deliberately jittered data and, depending on the application, a clean (jitter-free), sub-rate reference clock, eventually modulated for SSC. The data detected by the Rx is looped back through the I/O cell Tx and is checked by the BERT ED. Depending on the DUT architecture, the data looped back contains a certain portion of the jitter present on the stimulating data.

In most cases, the DUT Rx does not have a suitable clock output and the BERT PG clock signal itself cannot be used to clock the BERT error detector, because it may either be clean or, due to the Rx CDR limited bandwidth, only the lower frequency spectrum of the stimulated jitter is contained in the data looped back. Also, in case of SSC, the delays between the clock path to the error detector and the data looped back from the Rx don't match, closing the usable eye for the BERT ED (see Fig. 2) and causing possible erroneous detection on bits that may have been detected correctly by the Rx under test. Therefore, it is necessary to use a CDR in this measurement, which together with the BERT should correctly detect every bit supplied by the Rx under test, regardless of the data rate, the jitter, SSC content and the pattern itself. The test pattern has likely been selected as such that it stresses the Rx CDR; this is also extra stress for the BERT CDR, and the reason why it should feature built-in compensation for transition density.



Time:0.20UI/Div
Delay:-1.12UI
Scale:414.92mV/Div
Offset:-20mV

☑ 1e-6
☐ 1e-7
☐ 1e-8
☑ 1e-9
☐ 1e-10
☐ 1e-11
☑ 1e-12
☐ 1e-13
☐ 1e-14
☑ 1e-15

Sample Count	1-Level	0-Level	Rise Time	Fall Time	Eye Amplitude	Eye Height	Eye Width	Jitter Peak-Peak
2.212366E+09	843.36mV	-849.02mV	316.78mUI	308.00mUI	1.69V	1.47V	538.24mUI	461.75mUI

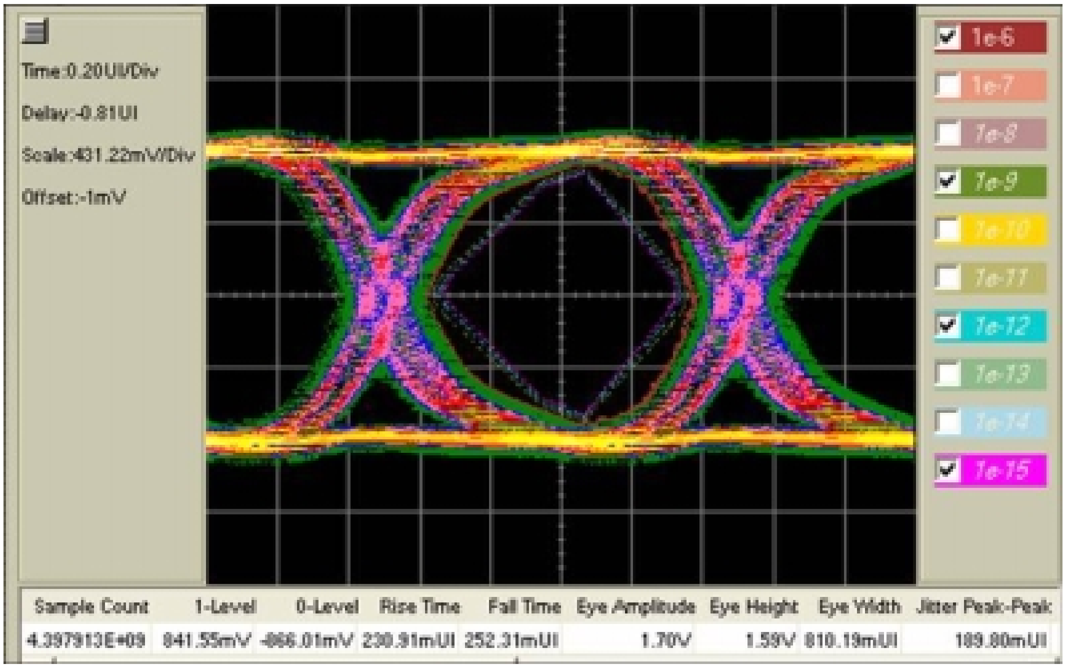
Fig. 2: Delays Causing Closed Eye

To simplify the test set-up and to eliminate potential uncertainties from the test set-up it is not only natural, but nearly mandatory, to integrate the CDR into the BERT ED. This CDR should work for all relevant data rates, have a bandwidth at least as high as that of the Rx CDR, and have compensation for different transition densities.

Tx testing: At first glance, oscilloscopes may be a more obvious choice than a BERT for Tx characterization, which can loosely be described as *waveform analysis*. Besides the fact that some BERTs are well suited for both signal eye- and mask-analysis, there is at least one parameter, total jitter (TJ), that only a BERT can truly measure -- and not only provide an *estimate* based on extracted values for deterministic and random jitter (DJ and RJ). The true measurement may be time consuming unless the BERT has a dedicated fast-TJ-measurement algorithm built in (see literature). However, to achieve a meaningful result, clocking of the BERT ED must have the same properties as the Tx system counterpart, the Rx, when in mission mode. As this usually comprises a CDR, certain portions of the Tx jitter spectrum are filtered and must not be accounted for TJ during waveform analysis, regardless if this is performed by a BERT or an oscilloscope. As described above, for the Rx jitter tolerance measurement, the bandwidth of the BERT CDR needs to be higher than that of the Rx under test. In terms of Tx measurements, the CDR parameters (not limited to bandwidth only) need to be matched to the target Rx-CDR parameters, and should be under user control, allowing analysis of their influence upon certain measurement results such as total jitter.

The CDR for Tx measurement may be an external (golden) PLL, but for each standard and data-rate a different PLL-unit would be required, or a versatile instrument with user-adjustable parameters such as bandwidth and peaking. It may seem natural to integrate it into the BERT ED, but in this case it is not only a question of convenience. With an external CDR the signal must be split externally or, provided the CDR has a splitter built in, at least routed through the CDR. In any case, splitting reduces the effective sensitivity of the BERT ED and the necessary cabling for routing through the CDR will distort the signal to be measured. ISI up to as much as 0.05UI maybe expected at 10G data rates -- a waste of margin that is no more available for the Tx. Furthermore, with an external CDR-unit, the delay between clock and data path must be optimized to minimize errors in the measurement result in the case of SSC.

This is where the Agilent J-BERT N4903A http://www.agilent.com/find/jbert comes into play by reducing the burden to create a measurement set up with sufficient performance since the problems of splitting and signal routing have already been solved by integration of the CDR into the BERT ED. The solution covers all relevant Gigabit data rates and applicable parameters, including the widely-adjustable bandwidth and peaking. Presets for popular standards are available in an integrated library, simplifying usage.



Time:0.20UI/Div

Delay:-0.81UI

Scale:431.22mV/Div

Offset:-1mV

Sample Count	1-Level	0-Level	Rise Time	Fall Time	Eye Amplitude	Eye Height	Eye Width	Jitter Peak-Peak
4.397913E+09	841.55mV	-866.01mV	230.91mUI	252.31mUI	1.70V	1.59V	810.19mUI	189.80mUI

Fig. 3: Eye Opened With J-BERT N4903A

About The Author

After receiving his Diploma in Electrical Engineering from the Ruhr University of Bochum, Germany, Michael Fleischer-Reumann joined Hewlett-Packard as an R&D engineer. He then became project leader for HP’s initial optical average power meter, attenuator and OTDR. Later, back at HP’s line of logic signal sources as an R&D project manager he led the development of the company’s first data generator analyzer system for physical-layer test, initial multiple serial BERT and initiated the first parallel BERT as a strategic product planner. His work resulted in several patents related to fiber optic components, electronic circuits and measurement methods.

During an eight-year period he lectured on electronics at the Stuttgart Berufsakademie, a college for engineers seeking Bachelor of Arts diplomas. Today, besides his position as Strategic Product Planner, Michael is active in standardization, contributing within IEEE and OIF, and his main technical interests are in the fields of signal integrity and jitter (tolerance) testing.

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